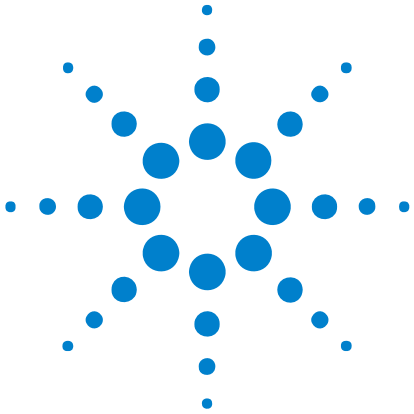

U4301 PCIe Gen3 Analyzer

Online Help

Agilent Technologies

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U4301 PCIe Gen3 Analyzer—At a Glance

The U4301 PCIe Gen3 analyzer lets you capture and decode PCI Express 3.0 (PCIe 3.0) data and view it in a Packet Viewer window. The protocol analyzer supports all PCIe 3.0 speeds, including 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2) through PCIe 8 GT/s (Gen3), and it supports link widths from x1 to x16.

The U4301 PCIe Gen3 analyzer is a blade installed in an Agilent Digital Test Console chassis (for example the U4002A portable 2-slot chassis).

When a controller PC is connected to an Agilent Digital Test Consol chassis via an external PCIe interface and cable, the *Agilent Logic Analyzer* application (running on the controller PC) lets you connect to the chassis, set up U4301 PCIe Gen3 analyzer data captures, and perform analysis.

The U4301 PCIe Gen3 analyzer provides:

Effective presentation of protocol interactions from physical layer to transaction layer:

- Industry standard spreadsheet format protocol viewer with:
  - Highlighting by packet type or direction.
  - Easy flow columns to better understand the stimulus and response nature of the protocols.
  - Context sensitive columns to show only the relevant information, minimizing the need to scroll horizontally.
- Flexible GUI configuration to meet debug needs, with pre-defined GUI layouts for Link Training debug, Config accesses, and general I/O.

Simple and powerful state-based triggering:

- New simple trigger mode makes it easy to setup single event triggers.
- Powerful state-based triggering including:
  - Four states supported in trigger sequencer.
  - Triggering on patterns (ordered set patterns or packet types).
  - Internal counters and timers.
  - Triggering on an ordered set on a specific lane.
- External trigger in/out.

Powerful hardware features ensure capture of important transition events:

- Dual phase lock loops (PLLs) per direction ensuring that the analyzer will lock on speed change events quickly and not miss any critical data.
- Large 4 GB of capture buffer per module (up to 8 GB of capture for x16 analyzer), for long recording sessions.
- PCIe Gen1 x4 link to the host PC, provides up to 10 Gbps of data download.

- LEDs to show lane status and speed for fast understanding of current link status.

See
- "Using the PCIe Gen3 Analyzer" on page 5

Using the PCIe Gen3 Analyzer

For an overview and list of features, see: "U4301 PCIe Gen3 Analyzer–At a Glance" on page 3

- Chapter 1, “Hardware and Software Installation,” starting on page 9
- Chapter 2, “Probing Options for PCIe Gen3,” starting on page 11
- Chapter 3, “Specifying the Connection Setup,” starting on page 13
- Chapter 4, “Setting the Capture Options,” starting on page 19
- Chapter 5, “Tuning the Analyzer for a Specific DUT,” starting on page 23
- Chapter 7, “Setting Up Triggers,” starting on page 39
- Chapter 8, “Running/Stopping Captures,” starting on page 49
- Chapter 9, “Viewing PCIe Gen3 Packets,” starting on page 51

For a printable version of this online help, see: *"U4301 PCIe Gen3 Analyzer Online Help"*.

See Also

- U4305 PCIeGen3 exerciser documentation.

Contents

1 Hardware and Software Installation

The U4301 PCIe Gen3 analyzer is a blade installed in an Agilent Digital Test Console chassis (for example the U4002A portable 2-slot chassis).

The Agilent Digital Test Console chassis is connected to a controller PC via a PCI Express Gen1 x4 interface and cable.

The controller PC runs the *Agilent Logic Analyzer* application software which lets you set up the U4301 PCIe Gen3 analyzer, specify triggers and other data capture options, capture data, and analyze the captured data using Packet Viewer windows.

See the *"Agilent Digital Test Console Installation Guide"* for information on:

- Installing the U4301 PCIe Gen3 analyzer blade into a Digital Test Console chassis.
- Connecting the Digital Test Console chassis to a controller PC via the PCI Express Gen1 x4 interface.
- Installing the *Agilent Logic Analyzer* software on the controller PC.

2 Probing Options for PCIe Gen3

The currently available options for probing a PCIe Gen3 device under test (DUT) are:

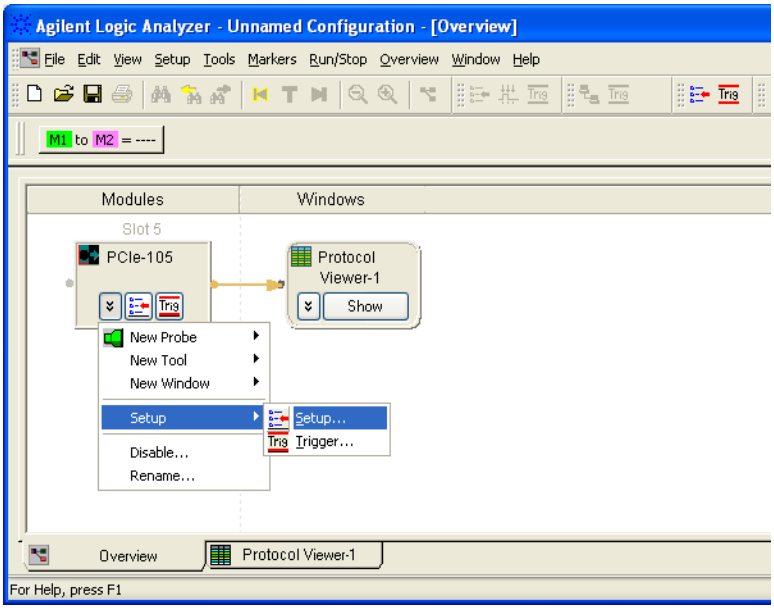
- The U4321A solid slot interposer.
- The U4322A midbus 3.0 probe.

Details about these two probing options (and other PCIe Gen3 tools) can be found in the the *"Hardware and Probing for PCI Express Gen3 User's Guide"*.

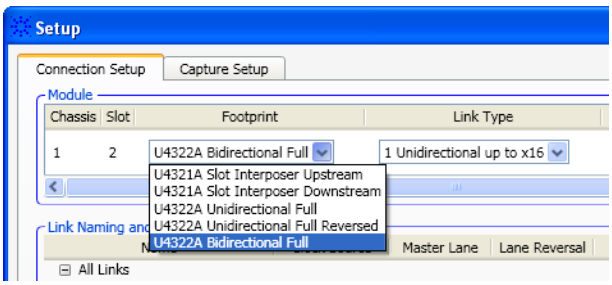
3 Specifying the Connection Setup

The first thing to do after connecting the *Agilent Logic Analyzer* application to the Agilent Digital Test Console chassis and U4301 PCIe Gen3 analyzer is to tell the application software how the analyzer is connected to the device under test. This is done in the Connection Setup tab of the analyzer's Setup dialog.

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Setup...**.



2 Specify the probing footprint type.



Upstream is the data direction toward the root complex.

Downstream is the data direction away from the root complex.

When used with the U4321A solid slot interposer, one U4301 PCIe Gen3 analyzer blade can probe either the upstream or downstream ports of the slot interposer. (It takes two U4301 blades to probe both upstream and downstream ports on the slot interposer.)

The U4322A midbus 3.0 probes require footprints to be designed into the device under test. Each probe requires its own footprint, and there are basically two variations:

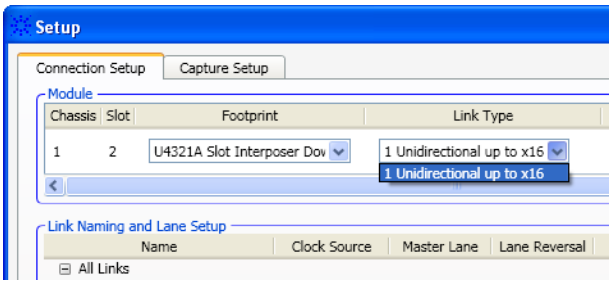
- *Bidirectional*– where half the footprint pins are for upstream data and the other half are for downstream data.
- *Unidirectional*– where all pins on the footprint are for data going the same direction.

Reversed refers to optional lane reversal which is supported for upstream ports.

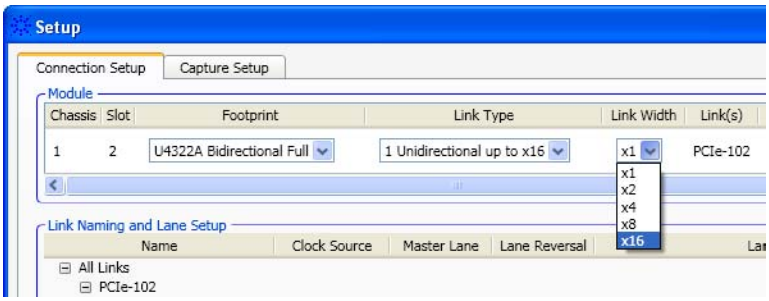
Whether all the pins on a U4322A probe are used (or whether multiple footprints are used) depends on the link width being probed.

For more information on probing, click **Connection diagram...** or refer to the *"Hardware and Probing for PCI Express Gen3 User's Guide"*.

3 Specify the link type.



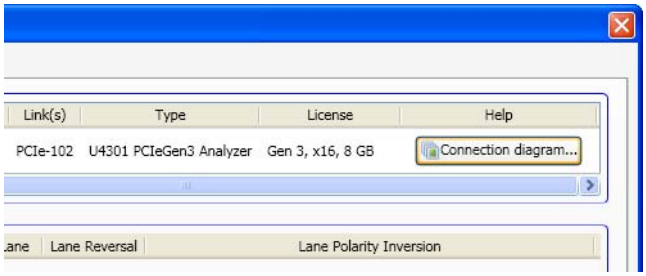
4 Specify the link width.



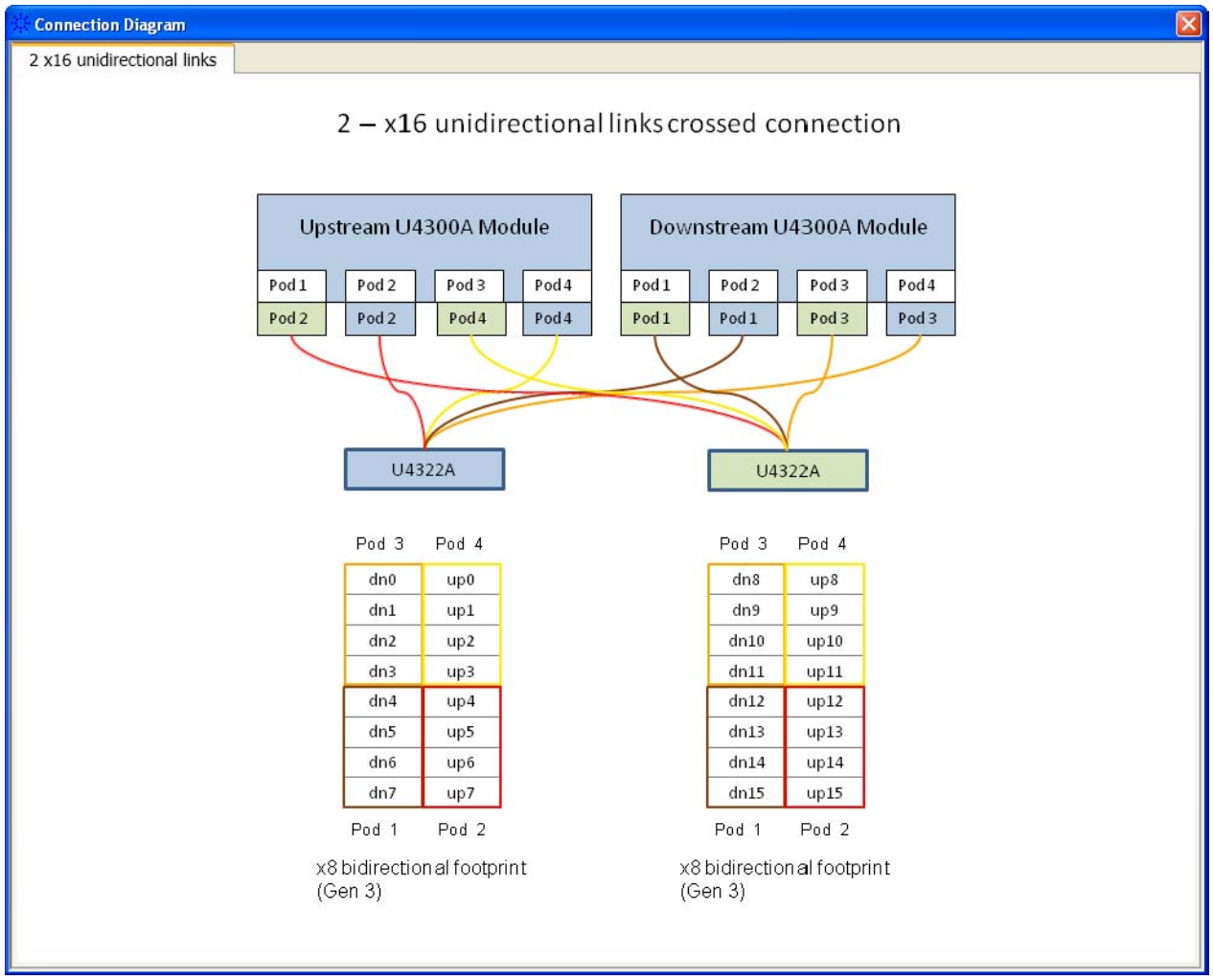
Select the link width that matches the negotiated link width of transmitter and receiver.

5 Verify the connection:

a Click **Connection diagram...**.

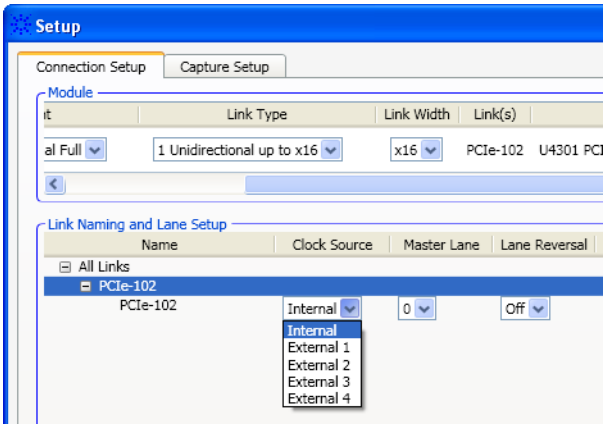


b Use the Connection Diagram dialog to verify that your connection setup specification matches the actual device under test connection.



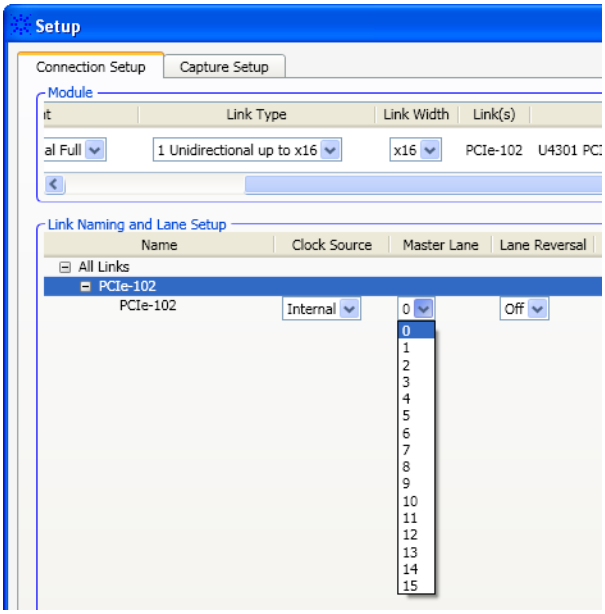
c Close the Connection Diagram dialog.

6 Select the clock source:

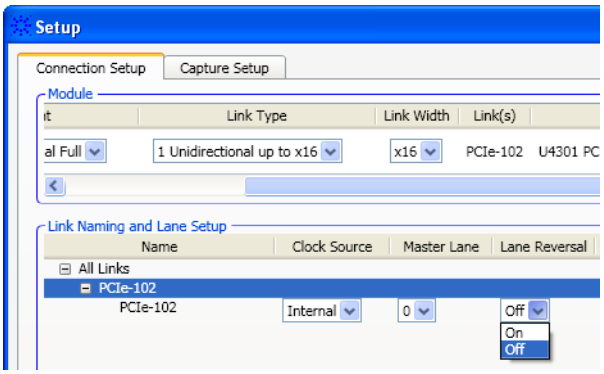


- **Internal** — selects an internal clock source. You should select Internal if the data rate is in the range of 2.5 Gbps or 5 Gbps +/-50 ppm. Note that there is no input clock in this mode.
- **External 1/2/3/4** — selects an external clock source. You should select External if the device under test uses SSC or the data rate is in the range of 2.5 Gbps +/-300 ppm (+0% / -0.5% if using SSC). The clock rate for external mode should be between 100 MHz +/-300 ppm (+0% / -0.5% if using SSC).

7 Select the master lane.



8 Specify whether lane reversal is on or off.

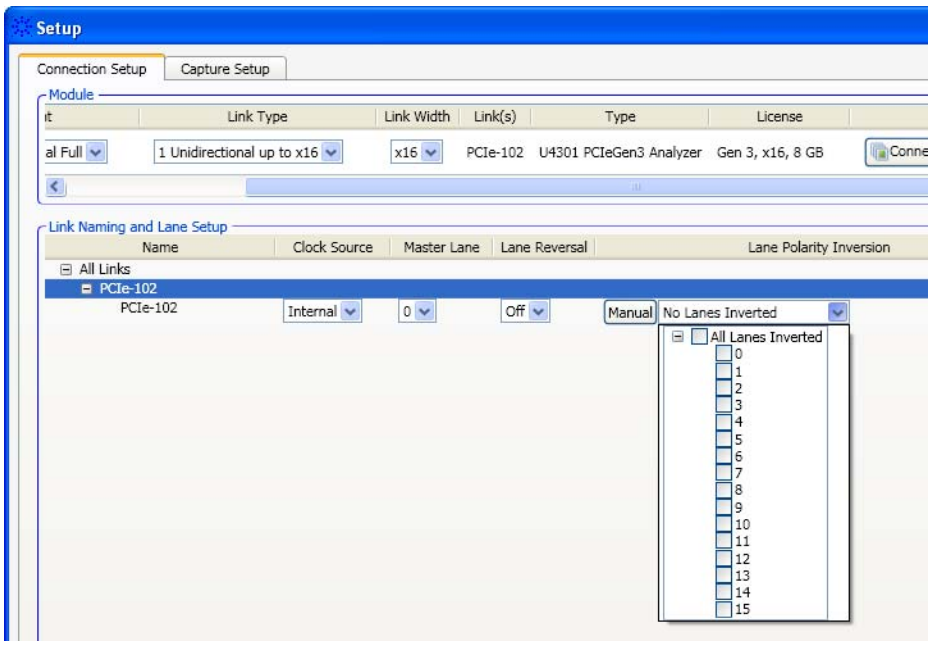


9 Specify any lane poalrity inversion:

a Click **Auto** or **Manual** to toggle between the types of polarity inversion specification.

When Auto is selected, the polarity of the lanes is set automatically during the initial link training.

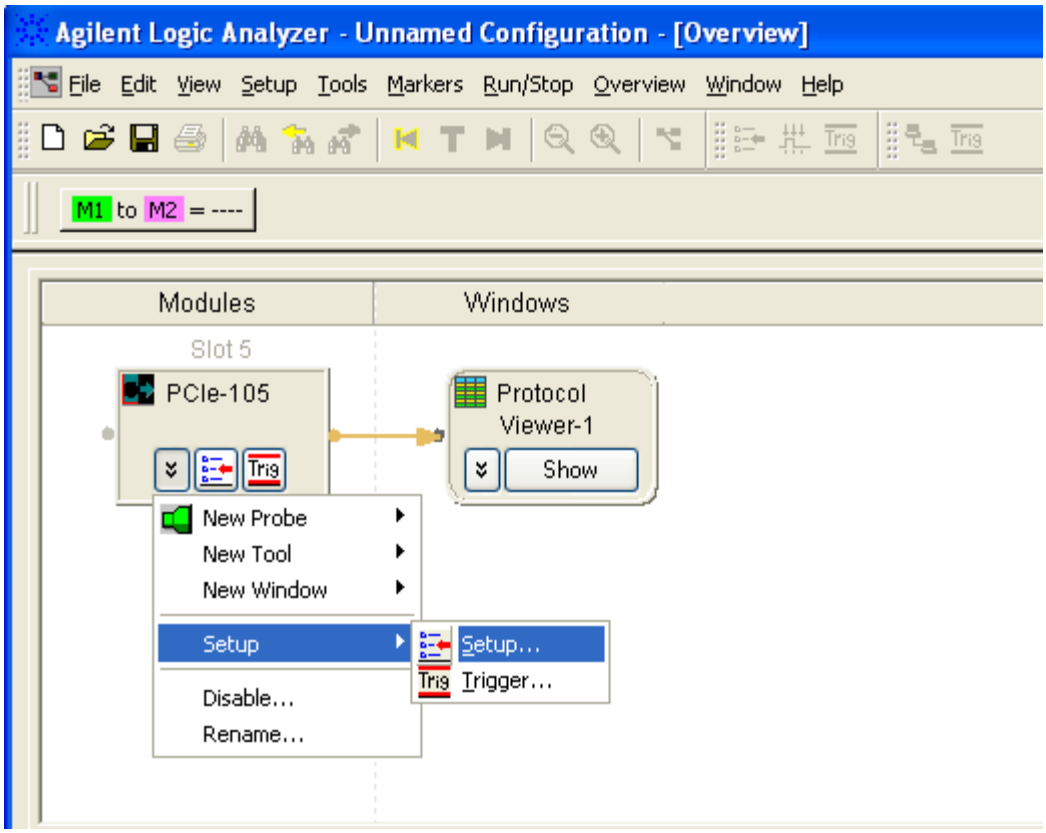
b When manual selection is chosen, select the lanes that are inverted.



4 Setting the Capture Options

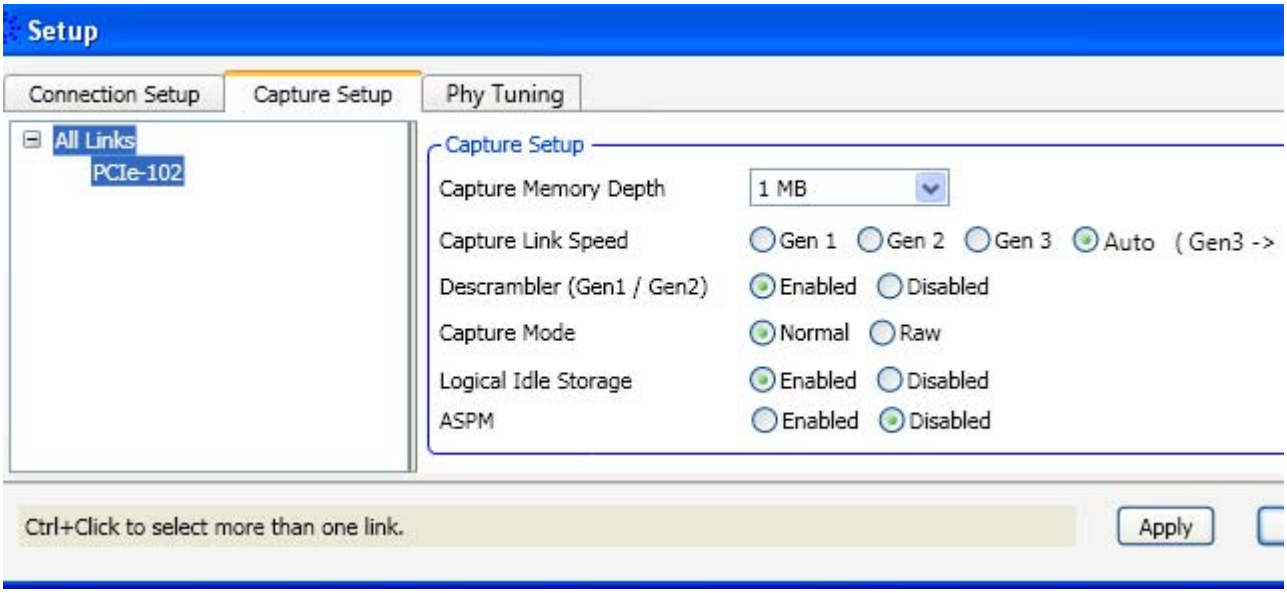
The Capture Setup tab in the PCIe Gen3 analyzer's Setup dialog lets you set basic capture options.

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Capture Setup** tab.

3 In the Capture Setup tab, select the appropriate options.



Capture Memory Depth	Lets you select the trace memory depth. Deeper traces capture more activity but take longer to save and process.
Capture Link Speed	Lets you specify the link speed of the data to be captured: • **Gen 1** — select this when capturing data on 2.5 Gbps links. • **Gen 2** — select this when capturing data on 5 Gbps links. • **Gen 3** — select this when capturing data on 8 Gbps links. • **Auto** – select this option when testing link speed switching scenarios. On selecting this option, analyzer automatically detects the link speed change and accordingly starts capturing data based on the changed link speed. The Auto option also has a drop-down listbox displayed with it. From this listbox, you can select either Gen1 or Gen2. If you select **Gen1** from this listbox, then analyzer prioritizes and captures the Gen 1 ordered sets while switching speed from Gen 3. If you select **Gen2** from this listbox, then analyzer prioritizes and captures the Gen 2 ordered sets while switching speed from Gen 3.
Descrambler (Gen1 / Gen2)	Tells the analyzer whether the descrambler algorithm is necessary: • **Enabled** — activates the descrambler algorithm. This algorithm generates the descrambled packet stream from an incoming scrambled packet stream. • **Disabled** — deactivates the descrambler algorithm. Select this option when the DUT is transmitting the non-scrambled data. Garbage data is displayed if this is set incorrectly.

Capture Mode	Lets you choose between two capture modes: • **Normal** — captures data only when all the configured lanes are out of the Loss of Sync (LOS) condition, that is, each lane has valid data. In this mode, channel bonding occurs when the analyzer encounters the first SKIP ordered set after exiting from the L0s/L1/L2/recover.speed condition. • **Raw** — captures data by each lane. This means, if only one lane is out of the LOS condition, its data is captured in the trace. In this mode, channel bonding may not exist at all. The Raw mode gives you data visibility even when there are significant PHY layer issues.
Logical Idle Storage	Specifies whether logical idles are stored in the capture: • **Enabled** — logical idles are stored. • **Disabled** — logical idles are not stored.
ASPM	Lets you control the ON/OFF of squelch detection circuitry. • **Enabled** — When you enable the ASPM option, the squelch detection circuitry is ON. In this case, power management capabilities are enabled and enhanced in terms of improvement in locking time and faster data capture while coming out of the electrical idle. • **Disabled** - When you disable the ASPM option, the squelch detection circuitry is OFF. In this case, power management capabilities are available but not enhanced.

NOTE

When testing L0s/L1, ensure that you:

- set manual lane polarity.

- select a fixed capture link speed instead of Auto speed.

5 Tuning the Analyzer for a Specific DUT

Tuning is the process of adjusting Agilent's probing system to remove the effects of different driving silicon, termination silicon (or other termination schemes), imperfect transmission paths, and the fact that the probes are not in the "ideal" location for receiving a high-speed signal (that is, at the end of the transmission path).

Furthermore, a PCIe Gen3 system will negotiate TX Linear Equalization, and you would like to have the largest eye possible. Tuning does not affect either the transmitter or the receiver; it is used only to increase the eye as seen by the analyzer. This process involves having the system/device-under-test transmit a well-understood signal (which consists mostly of Pcie Gen3 "Logical Idles") which the system then analyzes to determine the best (most open) eye as seen by the analyzer.

Tuning creates a Physical Tuning file (.ptu) which contains the information necessary to adjust the probing system for a specific device-under-test (DUT). At the 8 Gbps speed, you need to load that .ptu file into the protocol analyzer software to have the best possible eye at the analyzer. If you want to verify that you have the correct .ptu file, there is a verification program that can be run to analyze the eye quality without re-running the tuning algorithm.

For the first release of the Agilent PCIe Gen3 software, the tuning and verification programs run under the Tool Control Language (Tcl), outside of the main Agilent software.

The steps involved in tuning are:

1 "Installing Tcl" on page 25
2 "Preparing Your System for Tuning" on page 26
3 "Creating a Physical Tuning File" on page 27
4 "Selecting the Tuning File in the Protocol Analyzer GUI" on page 32

When changes occur to your system (new silicon, new connections, etc.), repeat beginning at step 2.

When changing hardware (maybe even after re-seating connectors!), you may want to verify that you do not need to re-tune to the new setup. To do this, see:

- "Verifying a Tuning File" on page 34

Installing Tcl

You only need to follow these steps once for each controller PC:

1. Get the ActiveState Tcl software:
   a. Go to "www.activestate.com".
   b. Use their search box, and search for the "Download ActiveTcl Community Edition".

      You might want to read the license agreement; note that Number 1 in the terms (as of 7/2010) is: You may use this Package for commercial or non-commercial purposes without charge.

   c. Download version 8.5.(something).
2. Run the downloaded program to install the software.
3. After installation, start a Command Prompt window and enter the following commands:

```
teacup install tcom

teacup install math::statistics
```

Next

- "Preparing Your System for Tuning" on page 26

Preparing Your System for Tuning

Perform these steps to prepare for tuning:

1 Attach the Agilent PCIe Gen3 analyzer to the device under test.

Follow the directions for your probing situation.

Take note of which probing system you have; you will need to know this to run the tuning program:

- U4321A solid slot interposer.

  Note that there are four connections on this interposer; the upper two are for the "To Upstream" path (assuming that the card plugged into the top connector of the interposer is the downstream side). The lower two connectors are for the "to Downstream" direction.

- U4322A soft touch midbus 3.0 probe.

  Note that there are several supported footprints that define what lanes are at specific physical connections.

2 If the Resource Bus connector is connecting two blades together (the connector at the left of the blades), remove the Resouce Bus Connector and do the tuning one blade at a time.

After you have tuned, you can reconnect the Resource Bus Connector without affecting the tuning.

3 Your system must enter L0 at Gen3 speed (8 Gbps).

4 Set up your system so that it is transmitting the following at 8 Gbps:

a Mostly Logical Idle packets (scrambled zeros).

b Skip Ordered Sets (optional for the tuning to work, but probably necessary for your system).

c Update Flow Control DLLPs (again, optional for the tuning process, but part of the PCIe Gen3 specification even when the link is idle).

d Your system cannot enter electrical idle; doing so will cause incorrect tuning.

5 Gather the following information about your system:

a The number of lanes in use (1, 2, 4, 8, or 16).

b Which lanes (if any) are inverted by the transmitter.

Next

- "Creating a Physical Tuning File" on page 27

Creating a Physical Tuning File

After you have prepared your system for tuning, you can create a Physical Tuning file (.ptu):

1 Exit the *Agilent Logic Analyzer* application if it is currently active.

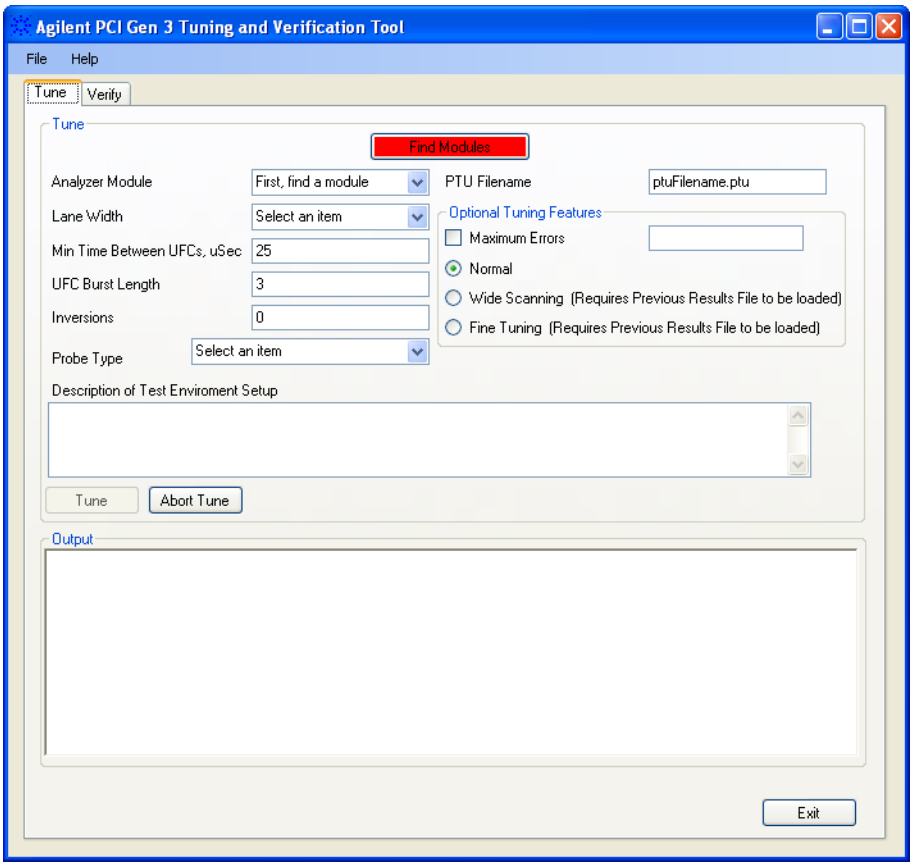
2 Start the *Agilent Logic Analyzer* application.

This is done to ensure that all of the default settings in the analyzer software are used.

You can iconify the *Agilent Logic Analyzer* application if desired.

3 Use the Windows Start menu to choose **All Programs > Agilent Logic Analyzer > Utilities > PCIe Gen3 Phy Tuning**.

4 Click the **Tune** tab.



5 Click **Find Modules**.

This detects valid modules and presents the Analyzer Module dropdown.

6 In the **Analyzer Module** dropdown, select the name of the module for which you want to create a tuning file.

This is the same module name you see in the *Agilent Logic Analyzer* application's Overview window. This is typically something like "PCIe- 102".

7 If you want to load the results of a previous tuning file to speed up the tuning this time, choose **File > Load Previous Results**.

8 Enter the appropriate options:

Lane Width	Is the number of lanes that your system is driving with Logical Idles (that is, the number of lanes that can be tuned). Should be 1, 2, 4, 8, or 16
Min Time Between UFCs, uSec	The minimum time between Update Flow Control DLLP bursts, in microseconds.. See: • "How "Minimum Time Between UFCs" and "UFC Burst Length" is Used in Tuning" on page 30 • "Understanding "Minimum Time Between UFCs" and "UFC Burst Length"" on page 29
UFC Burst Length	The number of back-to-back Update Flow Control DLLPs in a burst. This can be a number between 1 and 15. The default is 3. See: • "How "Minimum Time Between UFCs" and "UFC Burst Length" is Used in Tuning" on page 30 • "Understanding "Minimum Time Between UFCs" and "UFC Burst Length"" on page 29
Inversions	Is a set of 1's and 0's defining which lanes are inverted on your system as seen by the analysis connector. Lane 0 is always the last digit in the string. For example, if you have an 8-bit system, and lanes 0, 3, and 4 are inverted, INVERSIONS looks like 00011001
Probe Type	This is the type of probe that you are using to connect to your system. These include: • U4321A_To_Upstream — This is the top two connectors on the Slot Interposer. • U4321A_To_Upstream — This is the bottom two connectors on the Slot Interposer. • U4322A_Unidirectional_Full — This is the "midbus" probe, with all 16 lanes being transmitted by the same device. • U4322A_Unidirectional_Full_Reversed — This is the "midbus" probe, with all 16 lanes being transmitted by the same device. *Reversed* refers to optional lane reversal which is supported for upstream ports. • U4322A_Bidirectional_Full — This is the "midbus" probe, with 8 lanes being transmitted by one device, and the other 8 lanes being transmitted by a different device.
Description of Test Environment Setup	Enter a description of your test setup.

PTU Filename	This is the file that the tuning command will create; it stores the information about the test setup (lane inversions, number of lanes, etc) and the tuning parameters that were discovered during tuning. It is used both in the Probe Setup of the *Agilent Logic Analyzer* application and when verifying a tuning file (see "Verifying a Tuning File" on page 34). This file is stored at C:\Users\<CURRENT USER>\My Documents\Agilent Technologies\Logic Analyzer\SerialTuning\PCIe\PTU (Windows 7) or C:\Documents and Settings\<CURRENT USER>\My Documents\Agilent Technologies\Logic Analyzer\SerialTuning\PCIE\PTU (Windows XP), where CURRENT USER is the account currently logged in.
Maximum Errors	This is optional. If you have a target error rate in mind, you can use this to set the pass/fail criteria in terms of number of errors per bits tested.
Normal	This is the default tuning option.
Fine Tuning	This is optional. It is used to do "fine tuning" of the results of a previous tuning. This fine tuning can take quite a bit of time. Also, it starts with the results of the previous tuning, so the **Load Previous Results** option must be used! See also "Tuning Time vs Eye Quality at Analyzer" on page 31.
Wide Scanning	This is optional. It should only be used when the default tuning does not yield acceptable results. It essentially increases the "search space" for a tuning solution, and can thus take a very, very long time to run (several hours). You cannot use **Wide Scanning** and **Fine Tuning** for the same run.

9 Click **Tune**.

10 Now the tuning algorithm starts running.

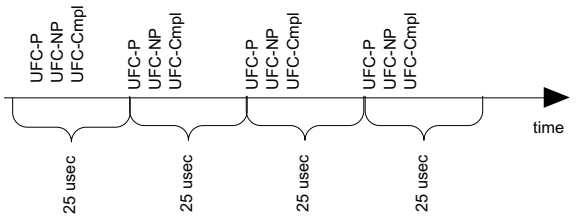
11 When the tuning algorithm finishes, the .ptu file you specified will be created.

Next • "Selecting the Tuning File in the Protocol Analyzer GUI" on page 32

Understanding "Minimum Time Between UFCs" and "UFC Burst Length"

The PCI Express specification calls on both upstream and downstream components to send out Update Flow Control packets with some maximum time between them. Generally, there are three UFCs per unit time: UFC-Posted, UFC-NonPosted, and UFC-Completions.

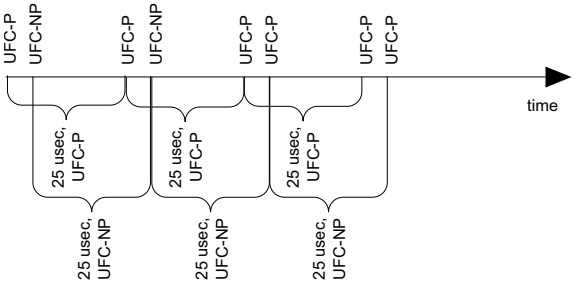
Sometimes the systems send out the UFCs in a "burst". For example, consider a system which, when the link is in Logical Idle, sends out UFCs every 25 micro seconds, and sends them out in a "burst". It might look like this on a graph of UFCs vs time:



For this example, the minimum time between UFCs would be 25 usec, and the UFC Burst Length would be 3.

Another example is where the UFCs come out seperated in time, but again have a time of 25 micro seconds between them.

In this example, no UFC-Completions are sent because the endpoint advertised infinite flow control credits. That might look like this:



For this example, the minimum time between UFCs would be 25 usec, and the UFC Burst Length would be 2.

It is probable that the timing is not exact; that is why the input is the "minimum time" between UFCs. So it is normal that for a system that intends to send out UFCs every 25 usec, you might enter 24 usecs.

See Also

- "How "Minimum Time Between UFCs" and "UFC Burst Length" is Used in Tuning" on page 30

How "Minimum Time Between UFCs" and "UFC Burst Length" is Used in Tuning

Tuning is done by looking at logical idle states in 8 Gbps mode (Gen3) and creating a Bit Error Rate Test based on the LFSR XOR'ed with 0's.

To get an accurate count, the non-zero data that normally occurs during a stream of logical idles — EDS TLLPs, SKP Ordered Sets, EIEOS, etc. — need to be detected and ignored. To reduce the dependency on an exactly correct protocol, a minimum number of dependencies on the protocol are used.

Update Flow Control packets are normally sent when a link is in the logical idle state. In order to ignore the "real" update flow control packets, but not demand that they be 100% correct, the tuning algorithm needs to know about how often they are sent.

If a value given the tuning alborithm is too small (that is, the UFCs are actually sent less often than the turning algorithm is told), the only thing that happens is that some errors that are signal integrity errors will be ignored; in this case, taking a trace after the tuning will show what the real time between UFCs are, and another tuning can be done with the correct values.

If the values given to the tuning algorithm is too high (that is, the UFCs are actually sent more often than the tuning algorithm is told), then some UFCs will be counted as signal integrity errors, and the tuning algorithm might take longer to complete and perhaps return suboptimal tuning. Again, in this case, after the tuning is performed a trace will show the correct timing between UFCs, and the next tuning can take that information into account to reduce the time to run and get more accurate results.

If there is no knowledge about the UFCs for a given target, enter small number for the time between UFCs – say 10 usecs – and "3" for the burst count (see "Understanding "Minimum Time Between UFCs" and "UFC Burst Length"" on page 29).

Tuning Time vs Eye Quality at Analyzer

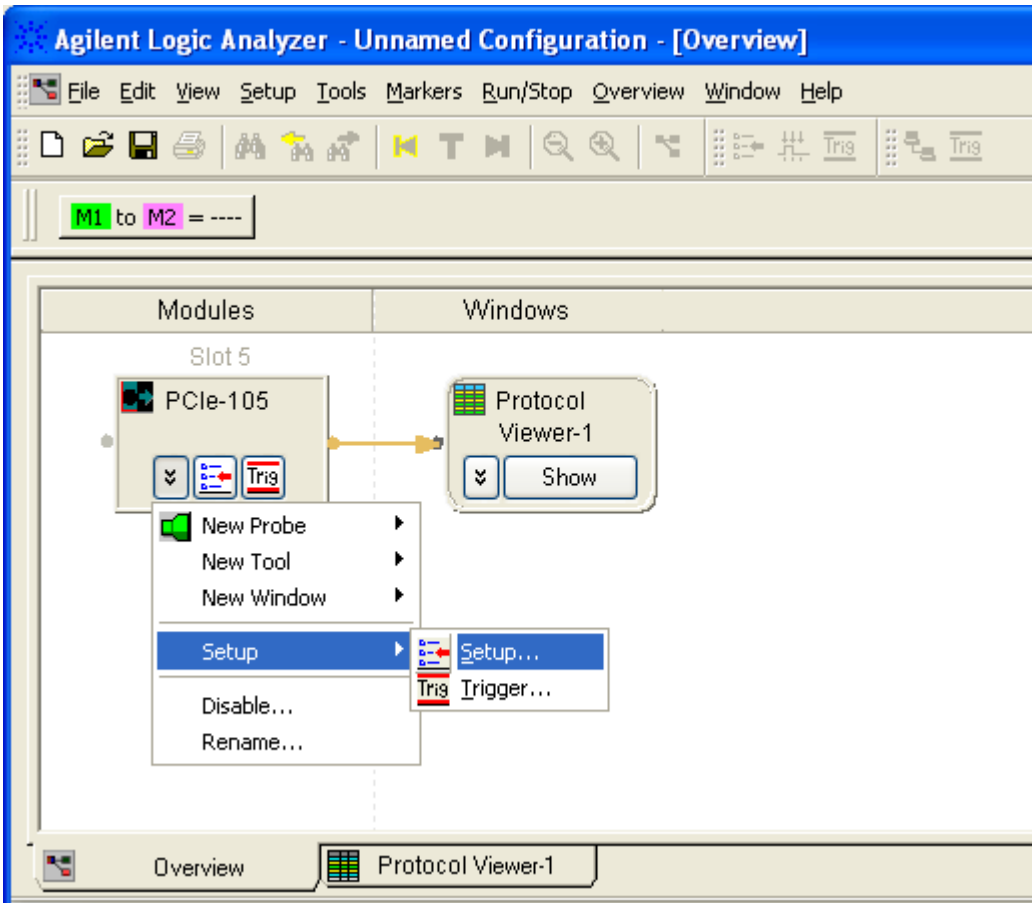
There is a trade-off between how long you want the analyzer to spend tuning its characterstics for a specific setup versus your needs. Depending on your analysis needs, you may choose to spend less time tuning in order to start analysis of your system quicker. Here is one way to think about it:

If you will be taking short traces, and the majority of time the data is being ignored, you can tune for a shorter period of time (and thus, potentially, tolerate a lower quality eye at the analyzer). Think about it in terms of the percentage of data you "care" about versus the percentage of data you don't care about, and the chance that (random) bit errors will occur during the time you are taking data.

Selecting the Tuning File in the Protocol Analyzer GUI

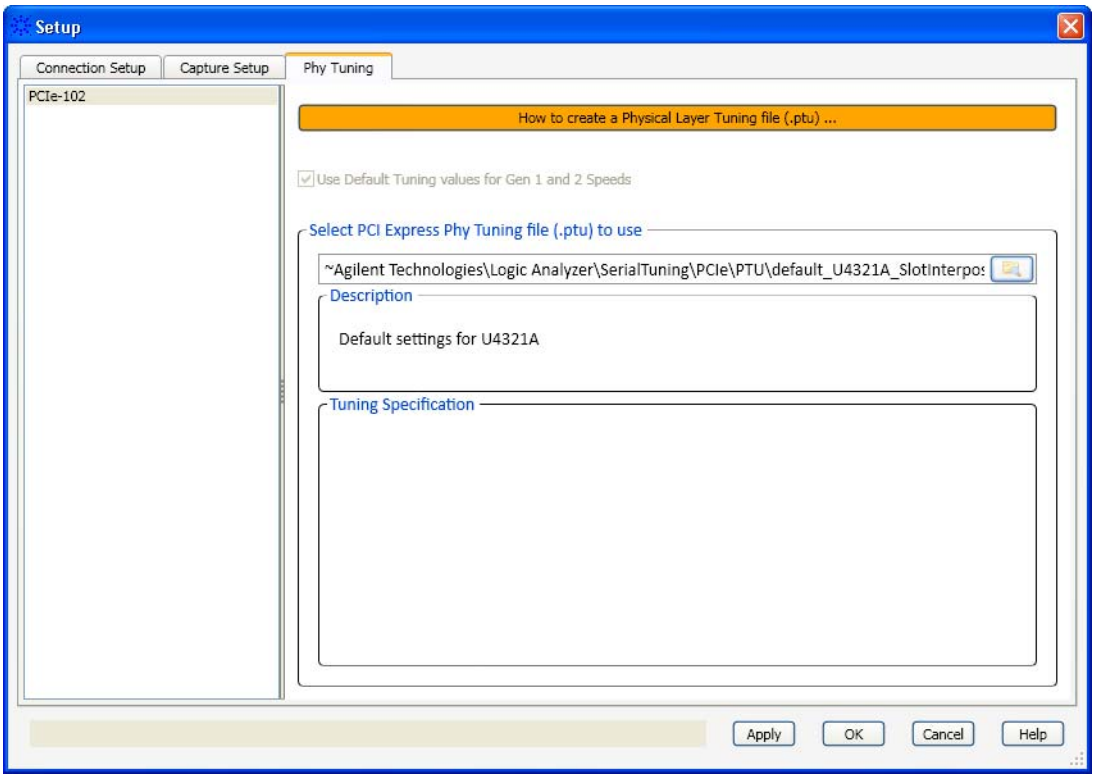
The Phy Tuning tab in the PCIe Gen3 analyzer's Setup dialog lets you set basic capture options.

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Phy Tuning** tab.

3 In the Phy Tuning tab, select the PCI Express Phy Tuning file to use.



4 Click **Apply** or **OK**.

Verifying a Tuning File

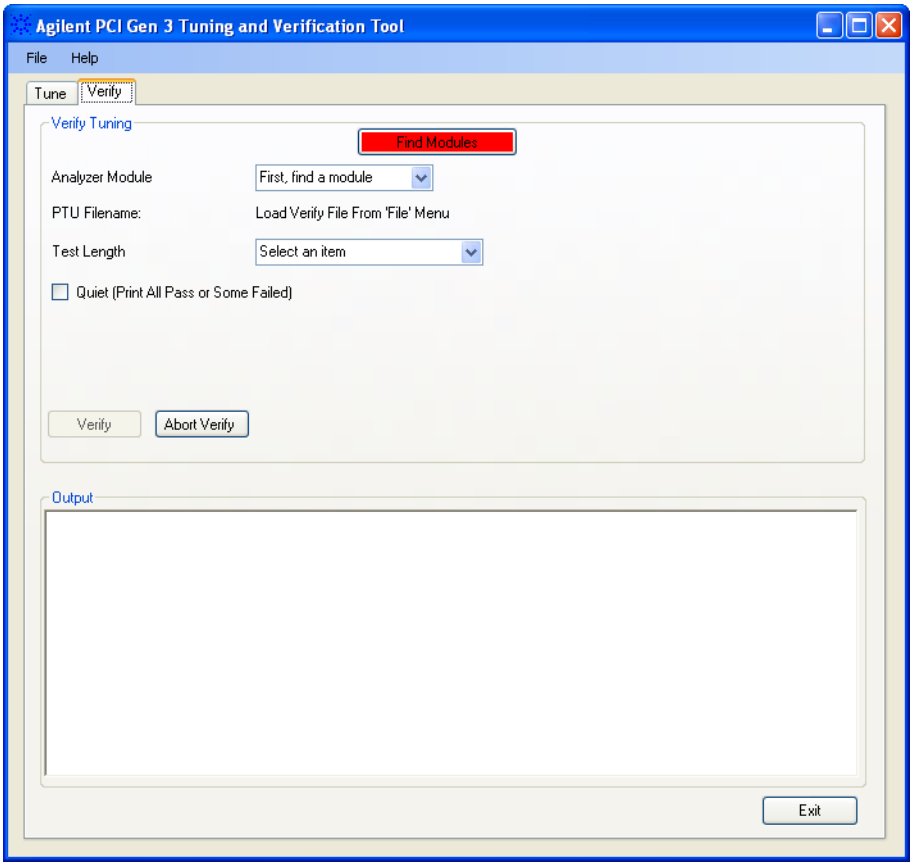
When changing hardware (maybe even after re-seating connectors!), you may want to verify that you do not need to re-tune to the new setup. To do this, you can verify a tuning file.

To verify a tuning file, you follow the same steps you did in order to create a tuning file. That is, install Tcl if this is a PC that you have not yet done that on, attach the PCIe Gen3 analyzer to your devce under test, and set up your system so that it is mostly transmitting Logical Idles (see "Preparing Your System for Tuning" on page 26). Then:

1. Exit the *Agilent Logic Analyzer* application if it is currently active.
2. Start the *Agilent Logic Analyzer* application.

   This is done to ensure that all of the default settings in the analyzer software are used.

   You can iconify the *Agilent Logic Analyzer* application if desired.
3. Use the Windows Start menu to choose **All Programs > Agilent Logic Analyzer > Utilities > PCIe Gen3 Phy Tuning**.
4. Click the **Verify** tab.



5 Click **Find Modules**.

This detects valid modules and presents the Analyzer Module dropdown.

6 In the **Analyzer Module** dropdown, select the name of the module that you want to verify tuning with.

This is the same module name you see in the *Agilent Logic Analyzer* application's Overview window. This is typically something like "PCIe- 102".

7 Choose **File > Load File to Verify Tuning**.

This is the file that the tuning command will verify.

This file is stored at C:\Users\<CURRENT USER>\My Documents\Agilent Technologies\Logic Analyzer\SerialTuning\PCIe\PTU (Windows 7) or C:\Documents and Settings\<CURRENT USER>\My Documents\Agilent Technologies\Logic Analyzer\SerialTuning\PCIE\PTU (Windows XP), where CURRENT USER is the account currently logged in.

8 Enter the appropriate options:

Analyzer Module	This is the name of the analyzer module as seen in the "Overview" window of the Logic Analyzer application. It is normally named "PCIe-101" or PCIe-102", but the user can change the name if desired.
Test Length	specifies how long the test will run. There are possible values: • about 3 seconds — about 10^{10} bits. • about 3 minutes — about 10^{12} bits). This is the default. • about 9 minutes — about $4*10^{12}$ bits.
Quiet	This is an optional command. If you have a target error rate in mind, you can use this to set the pass/fail criteria in terms of number of errors per bits tested.

9 Click **Verify**.

During the test, a seconds-counter will count down. It does not necessarily reach "0" before the number of bits tested have been observed (the counter is for a worst-case number of Skip Ordered Set blocks and Update Flow Control packets).

After the test is finished, a summary of errors is printed, which looks like this:

```
0: pass    1: pass    2: pass    3: pass    4: pass    5: pass    6: pas
s    7: pass
8: pass    9: pass   10: pass   11: pass   12: pass   13: pass   14: pas
s   15: pass
```

The summary of errors shows that lane 0 passed, lane 1 passed, etc.

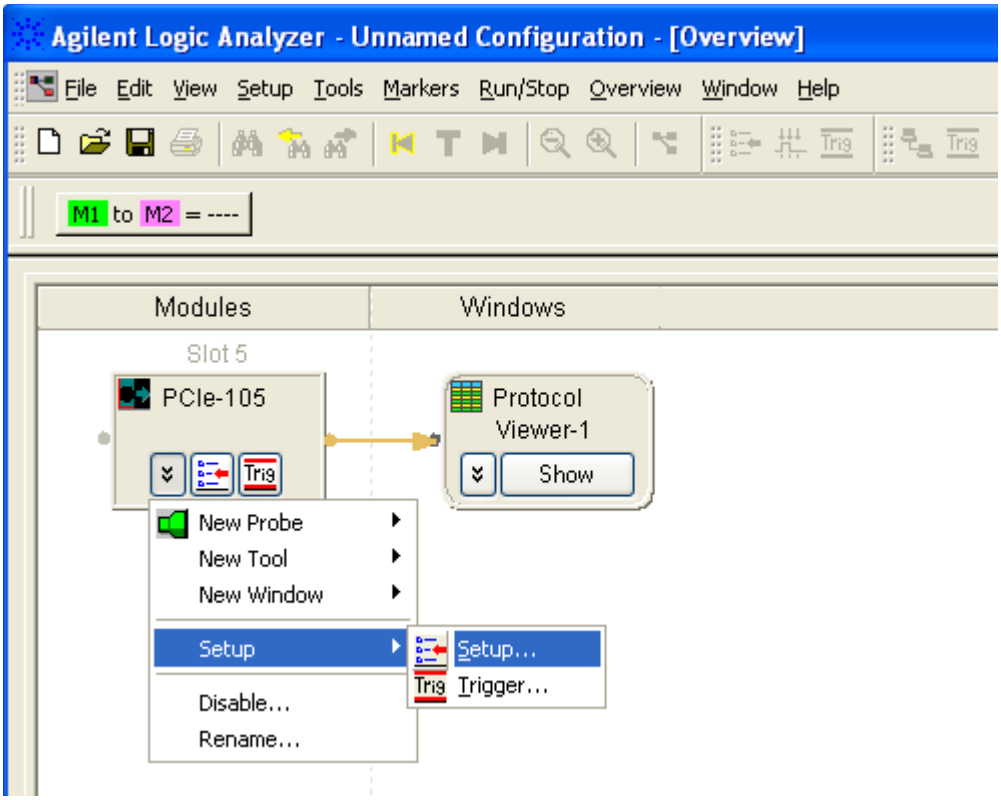
If any lane fails, make sure that Logical Idles are being transmitted on that lane. If they are, you should re-run the tuning algorithm on all lanes. (It does not take any more time to run tuning on all active lanes vs. a single active lane because the tests are all run in parallel.) You want to update the .ptu file for all active lanes.

6 Adjusting the Equalizing Snoop Probe (ESP) Settings

NOTE To enable the Probe Setup tab in the PCIe Gen3 analyzer's Setup dialog, you must check the Enable Advanced Probe Settings (ASP) option in the Options dialog. See "Options Dialog" (in the online help).

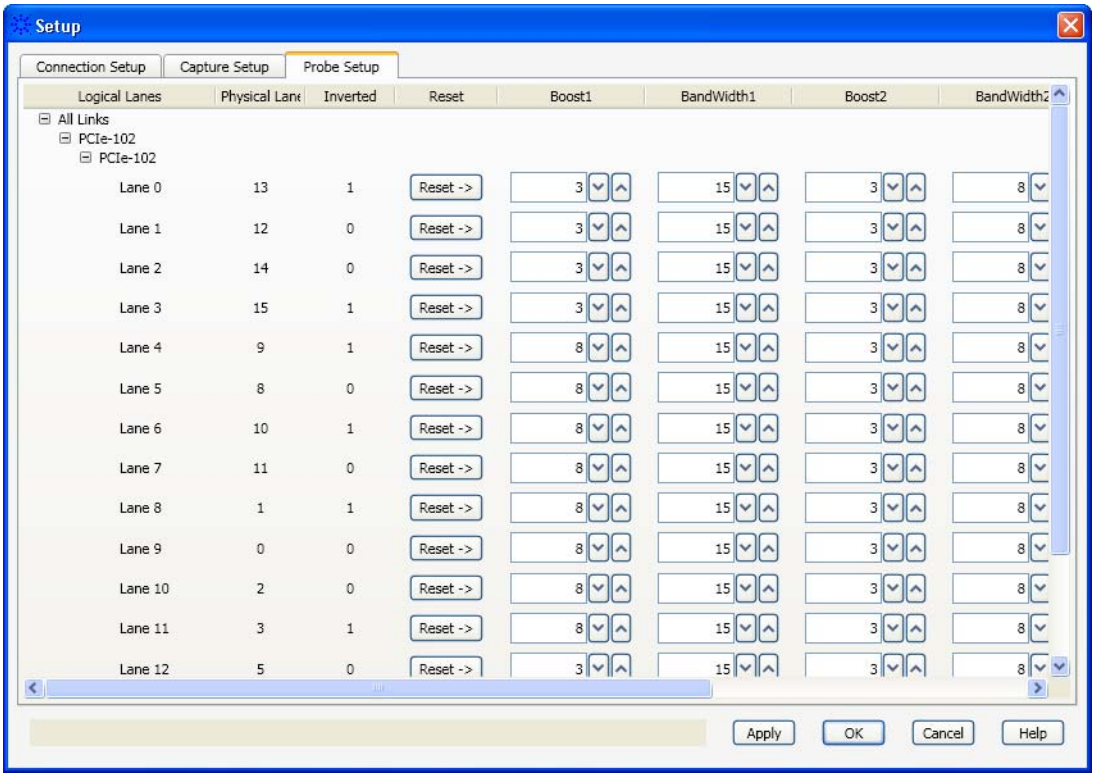
The Probe Setup tab in the PCIe Gen3 analyzer's Setup dialog lets adjust the equalizing snoop probe (ESP) settings.

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Probe Setup** tab.

3 In the Probe Setup tab, select the appropriate options.



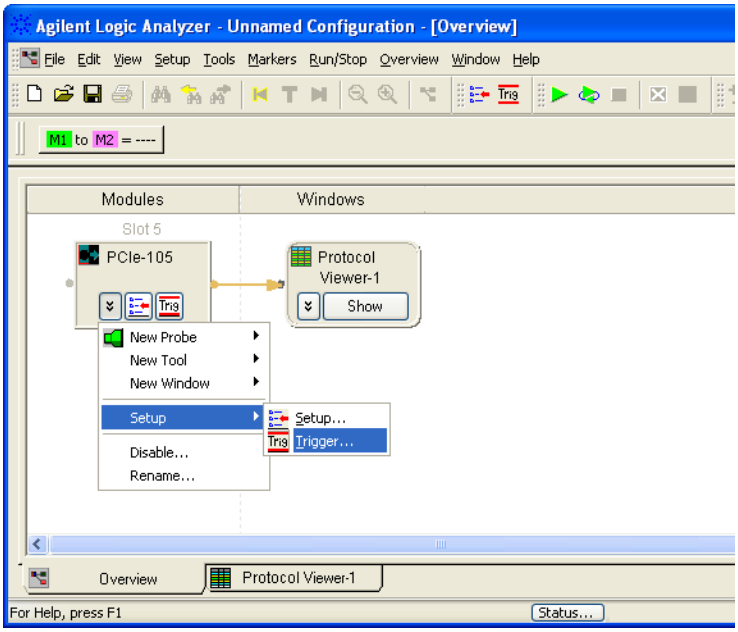
For each lane in the links, you can adjust the boost and bandwith settings. Click **Reset ->** to restore the original settings.

7 Setting Up Triggers

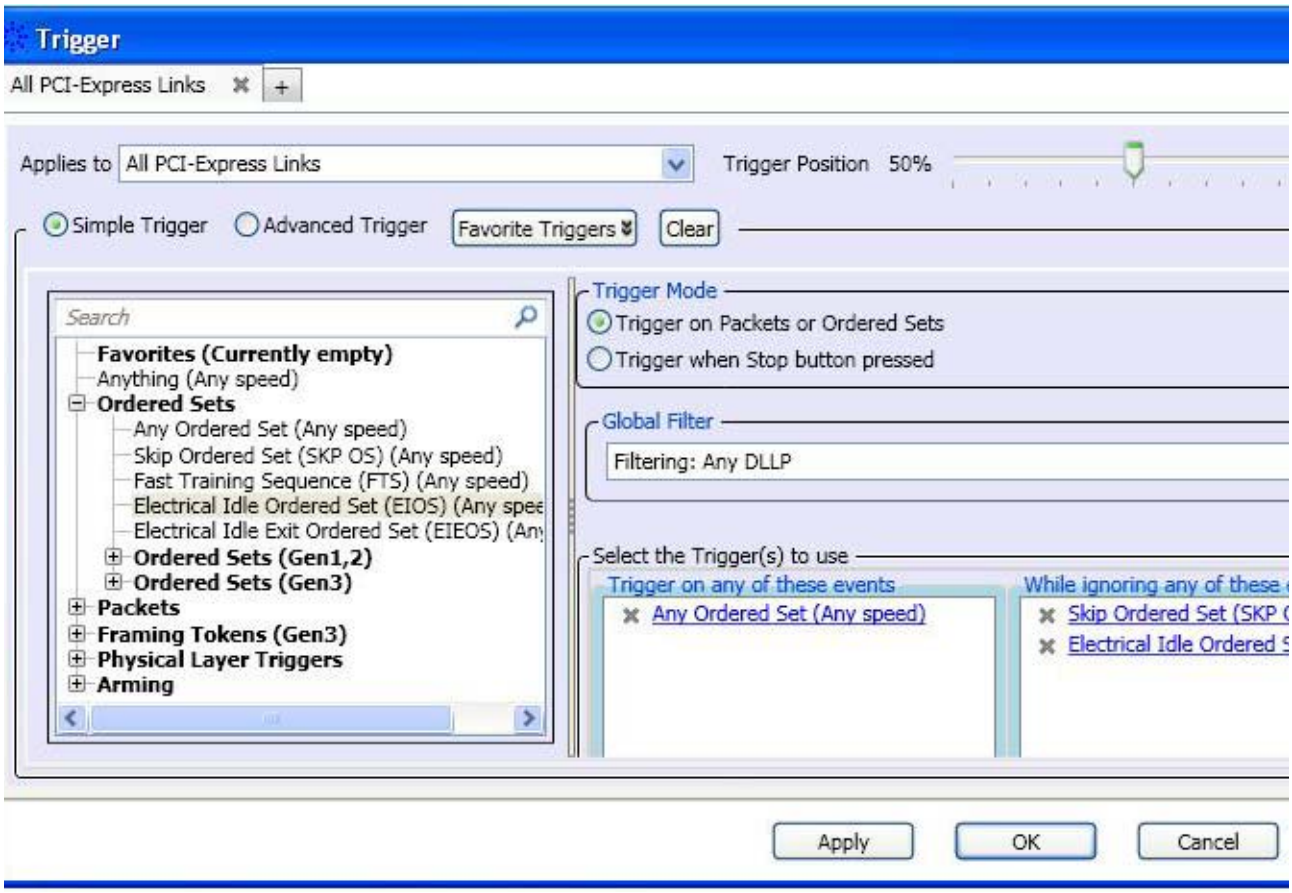
The U4301 PCIe Gen3 analyzer lets you set up triggers (events that specify when to capture a trace) with simple or advanced dialogs.

Setting Up Simple Triggers

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Trigger...**.



2 In the Trigger dialog:



a Select the **Simple Trigger** option.

b Select the **Trigger on Packets or Ordered Sets** Trigger Mode option.

(The **Trigger when Stop button is pressed** Trigger Mode option can be useful, for example, to see the events that lead up to a stop, halt, etc.)

c From the **Global Filter** listbox, select the types of ordered sets and TLP/DLLP packets that you want to filter out from getting stored in analyzer memory. The options selected from this list act as the storage qualifiers. The selected types of ordered sets and packets are acquired but are not qualified to be stored in the analyzer's memory. If you select the **Filter Everything** option from this list, then none of the acquired samples will qualify to be stored in the analyzer memory. As a result, analyzer will keep running and you need to stop it manually because analyzer keeps acquiring data until the memory depth is full. If you do not select any option from the list, then the filtering is considered Off and all the acquired data is stored in memory when the trigger condition is met.

d Drag events you would like to trigger on from the left-side pane to the **Trigger on any of these events** box.

The left-side pane contains an event hierarchy that can be expanded or collapsed.

To edit events in the trigger box, click the underlined event name.

To remove events from the trigger box, click the "X" to the left of the event name.

e Drag events you'd like to exclude from the trigger to the **While ignoring any of these events** box.

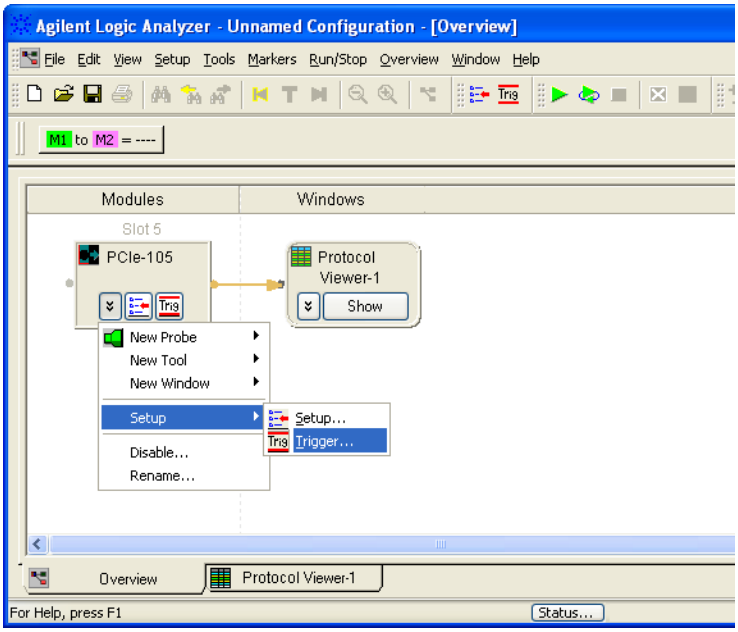
f Click **Apply** or **OK**.

See Also

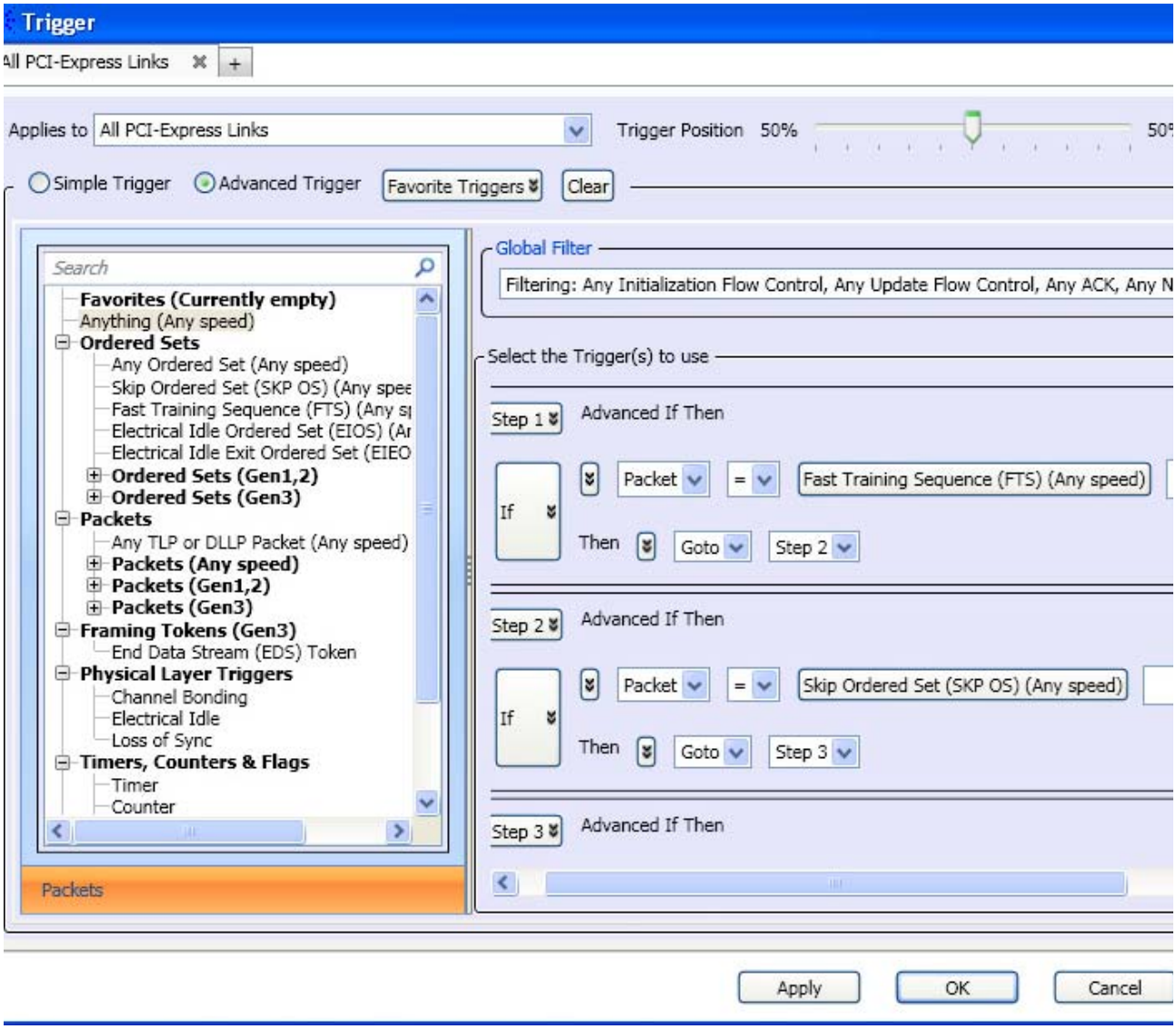
- "To select which links the trigger is for" on page 46
- "To set the trigger position" on page 46
- "To save/recall favorite triggers" on page 47
- "To clear the current trigger" on page 47

Setting Up Advanced Triggers

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Trigger...**.



2 In the Trigger dialog:



a Select the **Advanced Trigger** option.

b Drag events you'd like to trigger on from the left-side pane to sequence steps in the **Select the Trigger(s) to use** box.

The left-side pane contains an event hierarchy that can be expanded or collapsed. (This is the same event hierarchy displayed in the simple trigger dialog.)

To edit events in the trigger box, click the event button.

To remove events from the trigger box, click the sequence step buttons.

c In the **Select the Trigger(s) to use** box, click buttons, make drop-down selections, and enter values in fields to edit the steps in the trigger sequence:

- The **Step** buttons let you insert or delete steps.
- The **If**/**Else if** buttons let you insert or delete "if" clauses.
- The event chevron buttons let you insert, delete, or logically group (or negate) events.
- The action chevron buttons let you insert or delete actions.
- Use the **Comment** fields to document your advanced triggers.

d From the **Global Filter** listbox, select the types of ordered sets and TLP/DLLP packets that you want to filter out from getting stored in analyzer memory. The options selected from this list act as the storage qualifiers. The selected types of ordered sets and packets are acquired but are not qualified to be stored in the analyzer's memory. If you select the **Filter Everything** option from this list, then none of the acquired samples will qualify to be stored in the analyzer memory. As a result, analyzer will keep running and you need to stop it manually because analyzer keeps acquiring data until the memory depth is full. If you do not select any option from the list, then the filtering is considered Off and all the acquired data is stored in memory when the trigger condition is met.

e Click **Apply** or **OK**.

See Also

- "To select which links the trigger is for" on page 46
- "To set the trigger position" on page 46
- "To save/recall favorite triggers" on page 47
- "To clear the current trigger" on page 47

Setting General Trigger Options

The top part of the Trigger dialog contains general options that apply to both simple and advanced triggers.

To select which links the trigger is for

The top of the Trigger dialog has tabs that let you set up separate triggers for different links. You can add tabs for separate triggers and apply them to the links that are set up in the Connection Setup dialog (see Chapter 3, “Specifying the Connection Setup,” starting on page 13).

To set the trigger position

The top of the Trigger dialog has a slider for setting the trigger position within the capture memory.

Note that the pre-trigger portion of the capture memory is filled before searching for the trigger.

To save/recall favorite triggers

The top of the Trigger dialog has a **Favorite Triggers** drop-down menu for saving trigger setups and recalling previously saved trigger setups.

Do not confuse these "favorite" triggers with the favorites that appear in the left-side pane (which are added using the Event Editor dialog).

To clear the current trigger

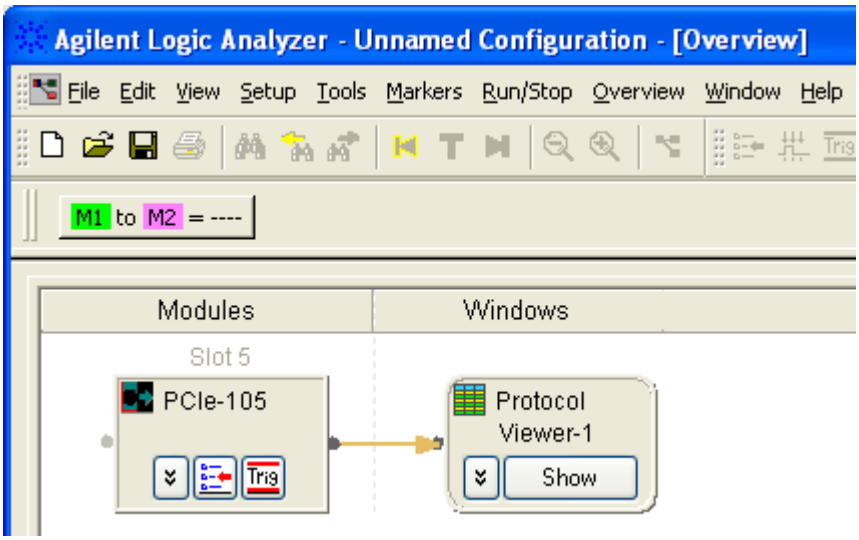
The top of the Trigger dialog has a **Clear** button for erasing the current trigger setup and restoing the default trigger setup.

8 Running/Stopping Captures

Running and stopping the U4301 PCIe Gen3 analyzer is just like running and stopping any other analyzer. See "Running/Stopping Measurements" (in the online help).

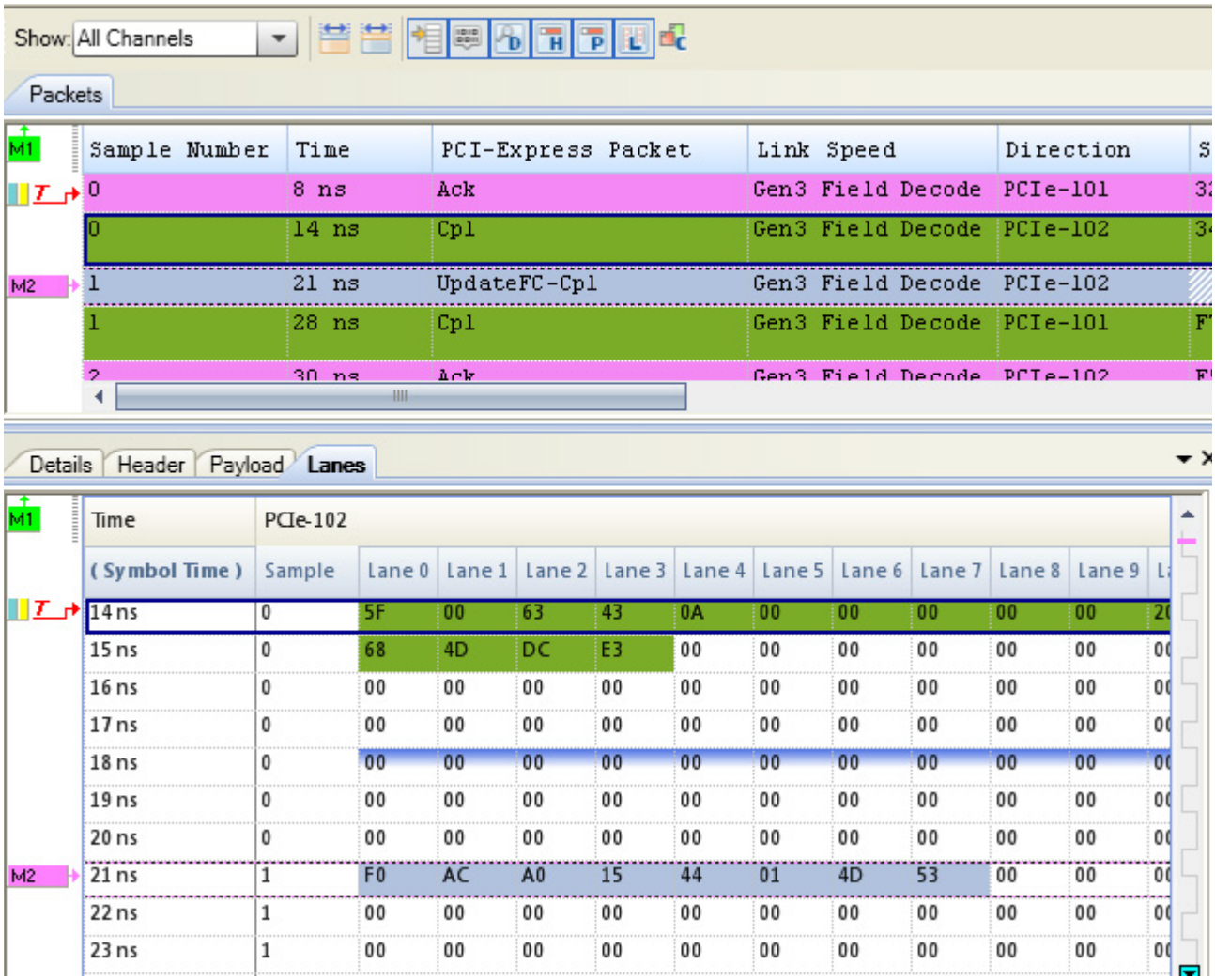
9 Viewing PCIe Gen3 Packets

Data captured by the U4301 PCIe Gen3 analyzer is viewed using the Protocol Viewer window. See "Analyzing Packet Data" (in the online help). A Protocol Viewer window is automatically added when you create a U4301 PCIe Gen3 analyzer module in the Logic Analyzer GUI.



The Protocol Viewer window displays the summarized and detailed packet information at the same time within two panes. The upper pane lists the packets. On selecting a packet, the details of that packet are displayed in the lower pane.

The following screen displays a sample view of the captured PCIe data in the Protocol Viewer window. In this screen, the Lanes tab of the Protocol Viewer window is displayed. The Lanes viewer displays not just the selected packet data across lanes but also the post packet data represented by colors matching the selected packet color in the upper pane.


Show: All Channels
Packets
Sample Number
Time
PCI-Express Packet
Link Speed
Direction
0
8 ns
Ack
Gen3 Field Decode
PCIe-101
0
14 ns
Cpl
Gen3 Field Decode
PCIe-102
1
21 ns
UpdateFC-Cpl
Gen3 Field Decode
PCIe-102
1
28 ns
Cpl
Gen3 Field Decode
PCIe-101
Details
Header
Payload
Lanes
Time
PCIe-102
(Symbol Time)
Sample
Lane 0
Lane 1
Lane 2
Lane 3
Lane 4
Lane 5
Lane 6
Lane 7
Lane 8
Lane 9
14 ns 0 5F 00 63 43 0A 00 00 00 00 00
15 ns 0 68 4D DC E3 00 00 00 00 00 00
16 ns 0 00 00 00 00 00 00 00 00 00 00
17 ns 0 00 00 00 00 00 00 00 00 00 00
18 ns 0 00 00 00 00 00 00 00 00 00 00
19 ns 0 00 00 00 00 00 00 00 00 00 00
20 ns 0 00 00 00 00 00 00 00 00 00 00
21 ns 1 F0 AC A0 15 44 01 4D 53 00 00
22 ns 1 00 00 00 00 00 00 00 00 00 00
23 ns 1 00 00 00 00 00 00 00 00 00 00

Glossary

D

DUT Device Under Test.

I

interposer Describes a probing method where the probe is located between a slot and the PCI Express device under test.

M

midbus probe Describes a probing method where Soft Touch footprints are designed into a DUT board between the controller and the device under test.

10 Glossary

Index

Index